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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,605	12/11/2003	Gary M. Johnson	2008.007900/03-0478	8519

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EXAMINER	
LE, DINH THANH	
ART UNIT	**PAPER NUMBER**
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,605	JOHNSON, GARY M.	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/16/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 25-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,10,25-28,33-38,43 and 44* is/are rejected.

7)☒ Claim(s) *5-8, 29-32 and 39-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 9-10, 35-38 and 43-44 remain rejected under 35 USC 103 (a) as being unpatentable over Lee (US 6,483,359) in view of Johnson et al (US 5,101,17).

Lee discloses in Figures 3-7 a DLL circuit used in a memory device (SRAM, lines 10-23, column 1) comprising:

- a phase detector (320) for comparing an reference clock signal (EXT_CLK) and a feedback signal;
- a coarse delay circuit (340) for switching an activation of a capacitive delay using switches (345-347, Figure 4);
- a fine delay (360); and
- a feedback delay unit (310).

However, Lee does not disclose that the delay circuit is a transitive capacitive delay.

Johnson et al suggests in Figures 3 and 4 a delay circuit comprising transitive capacitors (72a-72C) for easily implementing on an integrated circuit to reduce size since the size of the conventional capacitor is large.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the transitive capacitor as suggested by Johnson et al in the circuit of Lee for the purpose of reducing size.

Claims 1-4, 9-10, 25-28, 33-38 and 43-44 remain rejected under 35 USC 103 (a) as being unpatentable over Baker et al (US 6,445,231) in view of Lee (US 6,483,359)) and further in view of Johnson et al (US 5,101,17).

Baker et al discloses in Figures 1 and 12-15 a memory device comprising:

- a first device comprising a memory (102) and a DLL (111); and
- a second device (1502) coupled to the first device.

However, Baker does not disclose that the DLL circuit comprising delay circuit as recited in claim 1.

Nevertheless, Lee in view of Johnson et al suggests in Figure 1 a DLL circuit as stated above for providing a finer adjustability that would reduce jitter, see lines 5-9, column 1.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the modified DLL circuit of Lee in the circuit of Baker et al for the purpose of providing a finer adjustability that would reduce jitter.

Response to Applicant's Arguments

The applicant argues that the delay circuit of Lee is a passive device which does not activate a transistive capacitance delay. The argument is not persuasive because the delay circuits (340, 360) of Lee are active devices since they are switched capacitive delay circuits which are activated by the transitions of the gate voltages applied to the gates of the switches (345-347, Figures 4-5A). Moreover, employing the transistive capacitance delay circuits is suggested by Johnson et al., the circuits (71a-71c, 72a-72c), as shown in Figure 4.

The applicant argues that there is no motivation to combine the Lee reference with the Johnson et al reference or the Baker reference with the Lee reference and the Johnson reference. The argument is not persuasive because the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, i.e., Lee discloses a circuit with all of the limitations of the claimed invention as stated above with an exception of that the delay circuit is a transitive capacitive delay. While Johnson et al suggests in Figures 3 and 4 a delay circuit comprising transitive capacitors (72a-72C) for easily implementing on an integrated circuit to reduce size since the size of the conventional capacitor is large. Thus, employing the transitive capacitor as suggested by Johnson et al in the circuit of Lee for the purpose of reducing size would have been obvious to a person having skill in the art. Also, these references are analogous art because they disclose the delay circuits.

The applicant argues that Baker clearly does not disclose the delay circuit. The argument is not persuasive because the DLL circuit (111) of Baker includes delay circuits (1204-1207) as shown in Figure 12.

Allowable Subject Matter

Claims 5-8, 29-32 and 39-42 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The claims are allowed because the prior art does not suggest the delay circuit comprising the inverters and the transistor sets as combined in the claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/2/07